PATENT APPLICATION

DUAL PORT MEMORY CORE CELL ARCHITECTURE WITH MATCHED BIT LINE CAPACITANCES

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BACKGROUND OF THE INVENTION

Field of the Invention:

[0001] The present disclosure relates generally to the design and manufacture of Integrated Circuits (ICs). More specifically, the present invention relates to the design of Random Access Memory (RAM) ICs.

Description of the Related Art:

[0002] Semiconductor memory is typically laid out as an array of core cells, such that each individual core cell is coupled to a wordline and a pair of differential bitlines, as well as a power and ground connection. To read or write data from or to a selected core cell requires addressing circuitry for selecting the core cell, wordline drivers for driving the selected wordline and sense amplifiers for amplifying the signals that are read from the selected core cell and output buffers.

[0003] Fig. 1a is a simplified diagram of a memory 10 consisting of an array of core cells 12. Each of the core cells 12 is connected to a pair of bitlines, such as bitline (BL) 14 and a complementary bitline (/BL) 16. Each core cell is also electrically coupled to other core cells

12 along horizontal wordlines (WL) 18. Sense amplifying circuitry is usually implemented to read data, and write drivers to write data into selected core cells 12.

[0004] Although conventional sense amplifying circuitry has worked well in the past for sensing voltage differentials between the bitlines 14 and 16, higher performance memory now requires the ability to sense very small voltage differentials between the bitlines. Previously, sense amplifiers were required to sense voltage differentials of approximately 500 millivolts (mV) between the bitlines 14 and 16 to read data that was stored in a particular core cell 12. Due to expected fabrication imperfections and circuit layout constraints, there is usually a voltage offset between the bitlines 14 and 16. Voltage offsets are typically between 5 to 30 millivolts.

[0005] Although such offsets are typical, they were insignificant compared to the 500 millivolt voltage differential required for triggering amplification by a sense amplifier. However, higher performance memory now requires that amplification by the sense amplifier occur at much faster rates. Current sense amplifiers must respond more quickly and are required to sense voltage differentials of between about 15 and 60 millivolts across the bitlines. Unfortunately, typical voltage offsets in the range of 5 to 30 millivolts will necessarily begin to hamper the speed at which sense amplification may occur.

[0006] Fig. 1b shows a pair of exemplary bitlines 14 and 16 that are interconnecting successive core cells 12 in the vertical column direction. Also shown are representative wordlines 18 that horizontally interconnect each of the core cells 12. The core cells 12 are

typically symmetric data latching circuits that have cross-coupled inverters and passgate transistors that are coupled to respective wordlines 18. Although the core cells 12 are symmetric in their schematic circuit representation, the resulting geometric shape and layout orientation on a semiconductor substrate will usually be less than perfectly symmetric.

[0007] As a result, the capacitive loading experienced on each of the respective bitlines 14 and 16 will not be equal. When the voltage at point 32 is driven to rail voltage (V_{dd}), capacitive coupling of C_1 will occur between pre-charged transistors 30 and the bitlines 14 and 16. As pictorially shown in Fig. 1b, if the capacitive loading in the bitline 14 is "C+ ΔC" and the capacitive loading in the complementary bitline 16 is "C," then there will be a voltage offset of ΔV between bitlines 14 and 16 due to miller coupling capacitance. Other contributions to the offset are the result of process variation in the fabrication of the memory and different device size and strength. Bitline 14 may have a voltage of V and the complementary bitline 16 may have a voltage of V+ ΔV. It is this voltage offset that becomes problematic when voltage sensing between the bitlines is required at lower voltage differentials. This problem occurs while reading a low on complementary bitline 16, when the complementary bitline has a voltage of V+ ΔV.

[0008] Fig. 1c shows bitline 14 and the complementary bitline 16 graphed in terms of voltage and time, and illustrating that sense application will occur when accessing data of a particular core cell 12. In this example, the voltage offset is shown to be 15 millivolts (mV) between the bitline 14 and the complementary bitline 16. When sensing the digital data that is stored in this particular core cell, the complementary bitline 16 will begin to fall at time T_0.

The complementary bitline 16 must first cross the bitline 14 at time T_1. Therefore, a higher performance sense amplifier that is required to detect about 30 mV difference between the bitlines, and which must also cope with voltage offsets of 15 mV, will not commence its amplification until time T_3.

[0009] If there were no voltage offset between the bitlines as represented by a complimentary bitline 16', a sense amplifier would be able to sense a voltage differential of 30 mV much more rapidly at a time T_2. Thus, even very small voltage offsets have substantial performance deteriorating ramifications. Unfortunately, conventional memory device performance is limited by the expected fabrication imperfections and layout constraints that produce imbalances in capacitive loading of the bitlines of each core cell 12.

[0010] The design and fabrication of both static RAM (SRAM) with single and multiple ports and dynamic RAM (DRAM) is well known. A schematic of a known SRAM single port core cell is illustrated in Fig. 2. Core cell 20 is comprised of two inverters 21 the output of each inverter being coupled to the input of the other inverter. Inverters 21 store the binary "0" or "1" that forms the content of the core cell. Each core cell 20 is coupled to a pair of bit lines 23, which bit lines carry the data into and out of the core cell, and a word line 25, which word line indicates when it is asserted that either a new value will be written to core cell 20 or the contents of core cell 20 will be read. Access transistors 27 switch on to permit data placed on bit lines 23 to flow into inverters 21 of core cell 20 or out of core cell 20 onto the bit lines when core cell 20's word line 25 is asserted. This type of core cell is sometimes called a 6T cell, as it is fabricated from six transistors (each inverter 21 requires two transistors and the

two access transistors 27). The design and fabrication of core cell 20 and similar core cells are known to those of skill in the art.

[0011] Dual port SRAM core cells are also known. Fig. 3 is a schematic of a dual port core cell 50 that is very similar to the single port core cell illustrated in Fig. 2. In all figures referenced by this specification, similar parts have the same part number. The main differences between a single port and a dual port core cell are the provision of a second word line 29 and a second set of bit lines 31. The addition of second word line 29 requires an additional two access transistors 27 coupled to second word line 29, the bit lines 23 and 31 and the inverters. As with single port SRAM core cells, dual port core cells are known and their design and fabrication require no extensive description here.

[0012] A commonly used IC layout used to fabricate the dual port core cell shown in Fig. 3 is illustrated in Fig. 4. Approximately 2/3^{rds} of the cell's area comprises an n-type substrate 43 for the fabrication of n-type transistors and the other 1/3rd of the cell's surface area comprises a p-type substrate 45 for the fabrication of p-type transistors. These n-type and p-type transistors are then coupled together to form inverters 21. Trace 41 in Fig. 4 indicates the areas of the cell that are interconnected to form one of the inverters. Metal interconnections are run through and across the cell to various points, creating the bit lines, the word lines and the power and ground lines. The metal interconnections are not illustrated in Fig. 4

[0013] Although well known, dual port memory core cells laid out in the manner shown in Fig. 4 have certain performance limitations and problems. The height (indicated as "H" in Fig.

4) of these dual port memory core cells is great enough so that cumulatively the bit lines running to the transistors in a column of core cell have sufficient capacitance to affect the speed of the core cell materially. The bitlines are also typically closer together than is optimal, resulting in charge coupling between the bitlines, which reduces the speed of the core cell. Given the layout of known SRAM core cells, it is not possible to move the bitlines sufficiently far apart to eliminate this problem. Capacitance matching on the various bitlines is also difficult and limited space in the core cell prevents moving bitlines around to reduce this problem.

[0014] A core cell for either a dual port or single port SRAM memory with reduced height bit lines and reduced charge coupling on the bitlines would be a desirable improvement.

SUMMARY OF THE INVENTION

[0015] A core cell with an expanded layout is described herein as a preferred embodiment of the present invention. The cell is fabricated upon a three column substrate of N-type substrate, P-type substrate and N-type substrate. The core cell fabricated upon this three column substrate is reduced in height with respect to known core cells and only slightly wider than known core cells. The completed core cell is no larger in total area than known core cells and the wider but reduced height architecture allows for numerous advantages in the completed core cell.

[0016] Core cells fabricated using this preferred embodiment are reduced in overall height from known core cells, which in turn reduces the length of the bitlines running down a column of core cells. The reduced bit line height in the preferred embodiment in turn reduces the bit line capacitance, resulting in faster memory operation. The preferred embodiment also improves the internal capacitance balance as a result of improved matching of internal node capacitances permitted by the new architecture. The improved capacitance balance also improves overall memory performance.

[0017] The expanded architecture also greatly simplifies the placement and routing of the power lines and bitlines in the completed core cell. As will be shown in the detailed description of the preferred embodiments, the bitlines and their complement bitlines are separated by either ground lines or power lines. The separation of the bitlines and bitline complements eliminates capacitive coupling between these lines and also results in faster memory operation.

[0018] Core cells fabricated on a substrate fabricated according to the present invention are symmetrical in layout and can be flipped about their X and Y axis as needed to offset bitline and word line voltage mismatches. This new layout also permits vertical power lines, both V_{DD} and ground, which improves the power grid structure and also separates the bitlines. The separate power lines also permit simplified voltage biasing to reduce transistor leakage.

[0019] These and other aspects and advantages of the invention will become apparent from the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Fig. 1a is a diagram of a memory that has an array of core cells (Prior Art);

[0021] Fig. 1b illustrates a pair of exemplary bitlines that connect successive core cells in a vertical column (Prior Art);

[0022] Fig. 1c illustrates a bitline and a complementary bitline graphed in terms of voltage and time, illustrating transitions during sense amplification operation (Prior Art);

[0023] Fig. 2 is a block diagram of a known single port SRAM core cell (Prior Art);

[0024] Fig. 3 is a block diagram of a known dual port SRAM core cell (Prior Art);

[0025] Fig. 4 is a top down perspective of the silicon layout of the known dual port memory cell of Fig. 3 (Prior Art);

[0026] Fig. 5 is a top down perspective of the silicon layout of a first embodiment of the present invention; and

[0027] Fig. 6 is a top down perspective of the silicon layout of a first embodiment of the present invention, with the metalization layers illustrated.

Detailed Description of the Preferred Embodiments

[0028] Figs. 1a, 1b, 1c, 2, 3 and 4 have already been described and discussed as the relevant background to the present invention. They require no further discussion here.

[0029] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

[0030] Fig. 5 illustrates the final device layout of a core cell fabricated according to the first embodiment of the present invention. Core cell 100 is fabricated upon a substrate of first n-type substrate 101, first p-type substrate 103 and second n-type substrate 105. Two pnp transistors 107 are fabricated on substrate 103 and 6 npn transistors 109 are fabricated on substrates 101 and 105. The process steps required to fabricate these transistors are known and require no further description here. Black areas in Fig. 5 indicate where a via has been made from the various overlying metal layers (see Fig. 6), which form the ground, V_{DD} and bitlines, into the diffusion layer or polysilicon layer of the underlying transistors. The formation of these vias is conventional and does not require discussion here.

[0031] The schematic diagram of memory core cell 100 (Fig. 5) would be identical to that shown in Fig. 3. The processes used to fabricate memory core cell 100 are known in the art and require no discussion here.

[0032] As shown in Fig. 6, the two sets of bitlines are shown as bitline A, bitline /A, bitline B and bitline /B. Wordline contacts 111 turn on the passgate transistors when core cell 100 is addressed for reading or writing. V_{dd} contacts 113 and ground contacts 115 indicate where voltage and ground are provided to core cell 100. Like the bitlines, these lines run parallel to one another, as well as parallel to the bitlines, down the columns of core cells (see Fig. 1a). This arrangement of the bitlines, power lines and ground lines, which is only allowed by the unique layout of the present invention, effectively shields the bitlines from one another, which greatly reduces charge coupling caused by the signals on the bit lines. This architecture allows both faster reading from and faster writing to core cells constructed according to the present invention. The vertical power and ground lines also improves the power grid structure.

[0033] Current IC design processes first propose a layout for the IC design and then use modeling software to determine its performance. When a model appears to indicate that a design will perform as required, test ICs are fabricated and their actual performance measured against the expected performance. The process repeats iteratively both at the modelling and at the fabricate and test stages until performance specifications are met. The architecture of this first embodiment of the present invention permits this iterative design process to produce an optimized design more easily than known cell architectures, especially in terms of balanced bit line capacitances as well as balanced internal node capacitances. The increased width and reduced height provide more effective space for varying the size and positioning of the core cell's active devices to obtain the optimal results.

[0034] The core cell of this embodiment of the present invention tiles well, as its symmetrical layout permits core cells to be flipped and rotated to offset bitline and word line voltage mismatches as necessary as the number of core cells in each column of the memory increases.

[0035] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is: